ABSTRACT

A vector editor for providing an integrated circuit datapath layout. For one aspect, vectors may be extracted from an integrated circuit design input file using a name-based vector extraction approach, a bus/connectivity-based vector extraction approach or another approach. Each vector may be represented as one of a row and a column, wherein the representation differs from that of the associated physical layout. Each bit slice associated with the integrated circuit layout is represented in an orthogonal manner to the vectors. For one aspect, instances of similar master cells may be represented using similar visual representations.